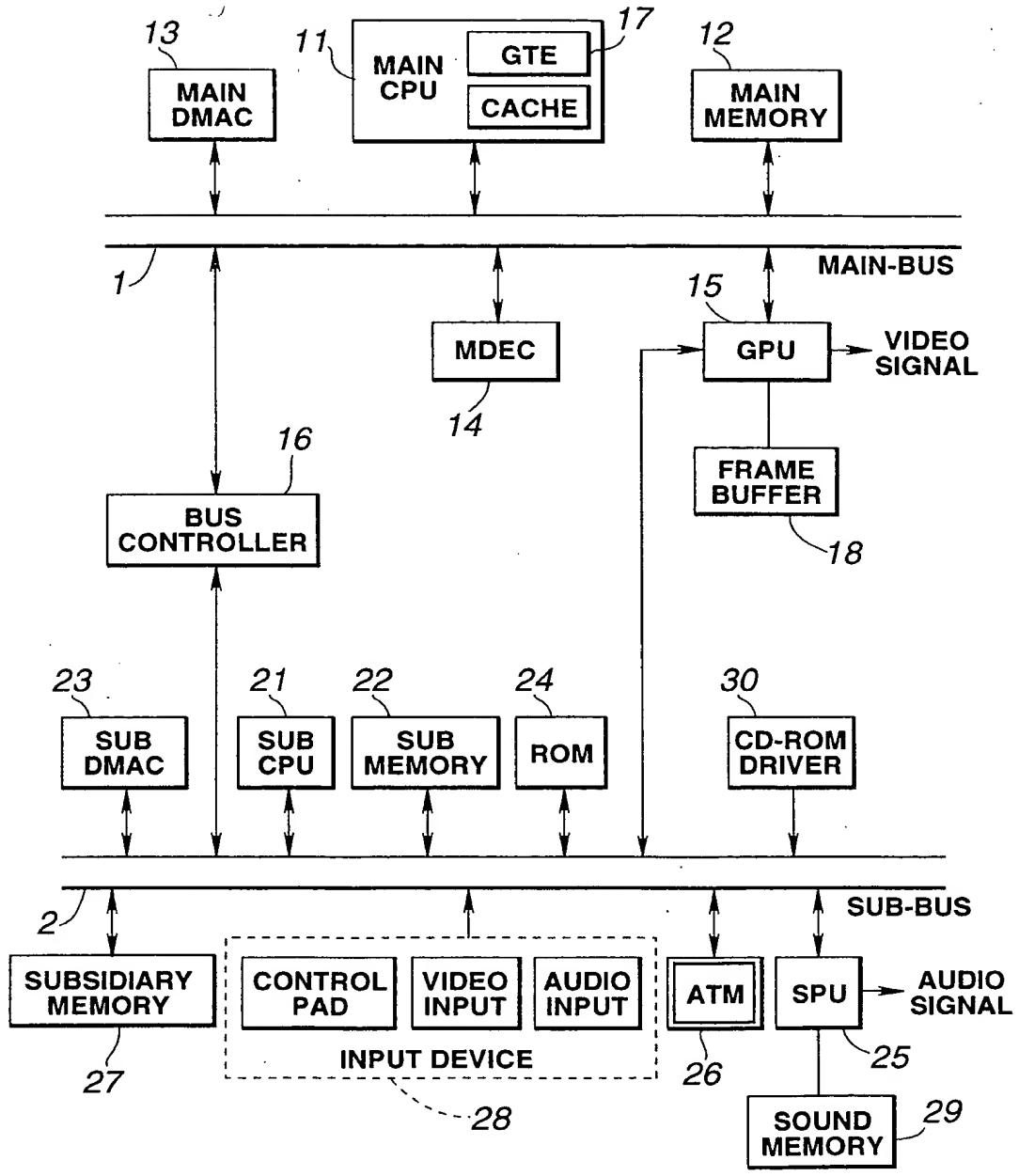
13
MAIN DMAC
11
MAIN CPU
GTE
CACHE
17
12
MAIN MEMORY
1
MAIN-BUS
15
MDEC
14
GPU
VIDEO SIGNAL
16
BUS CONTROLLER
FRAME BUFFER
18
23
SUB DMAC
21
SUB CPU
22
SUB MEMORY
24
ROM
30
CD-ROM DRIVER
2
SUB-BUS
SUBSIDIARY MEMORY
27
CONTROL PAD
VIDEO INPUT
AUDIO INPUT
INPUT DEVICE
28
ATM
26
SPU
AUDIO SIGNAL
25
SOUND MEMORY
29

FIG.1

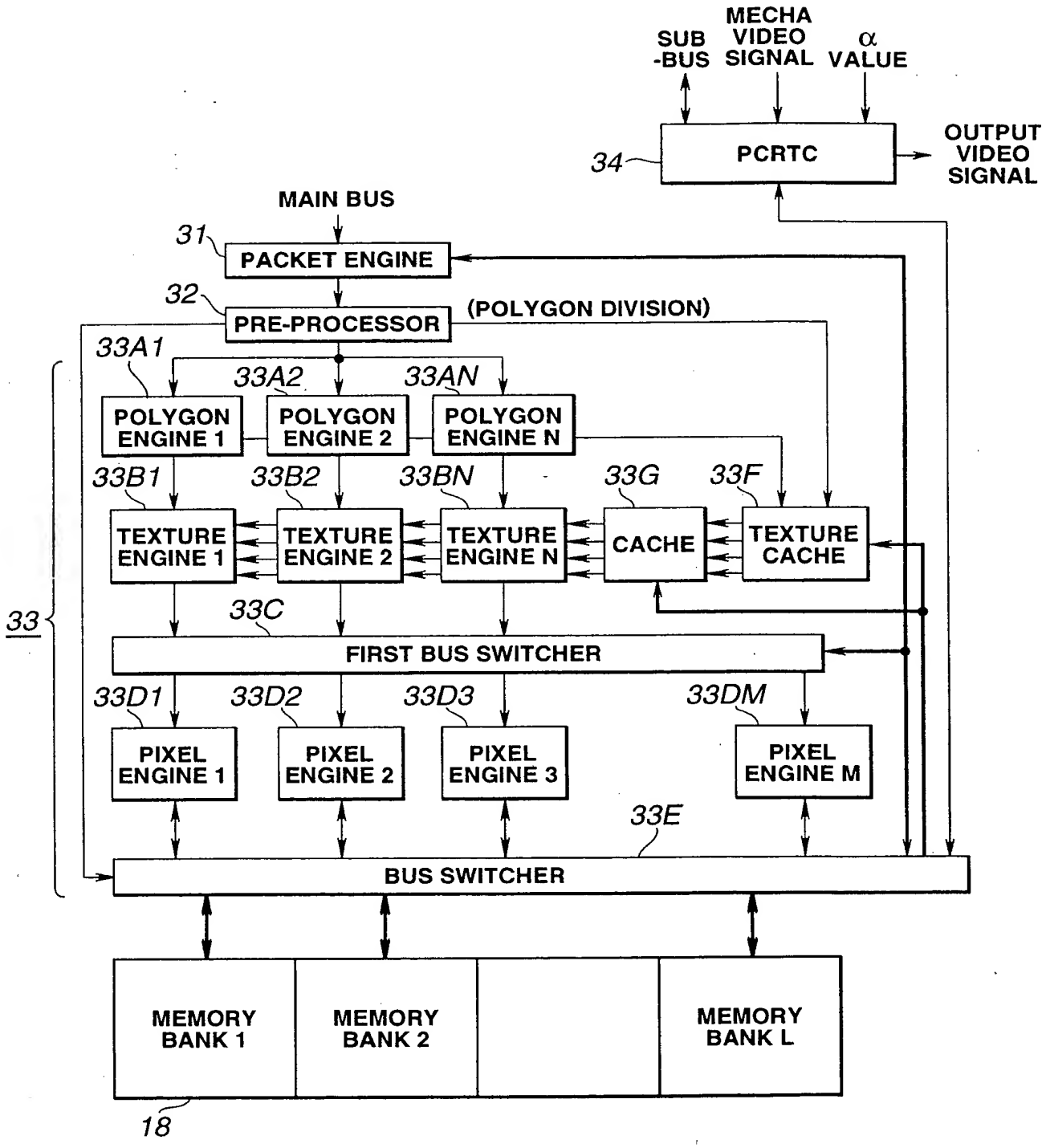
SUB -BUS
MECHA VIDEO SIGNAL
α VALUE
34
PCRTC
OUTPUT VIDEO SIGNAL
MAIN BUS
31
PACKET ENGINE
32
PRE-PROCESSOR
(POLYGON DIVISION)
33A1
33A2
33AN
POLYGON ENGINE 1
POLYGON ENGINE 2
POLYGON ENGINE N
33B1
33B2
33BN
33G
33F
TEXTURE ENGINE 1
TEXTURE ENGINE 2
TEXTURE ENGINE N
CACHE
TEXTURE CACHE
33
33C
FIRST BUS SWITCHER
33D1
33D2
33D3
33DM
PIXEL ENGINE 1
PIXEL ENGINE 2
PIXEL ENGINE 3
PIXEL ENGINE M
33E
BUS SWITCHER
MEMORY BANK 1
MEMORY BANK 2
MEMORY BANK L
18

FIG.2

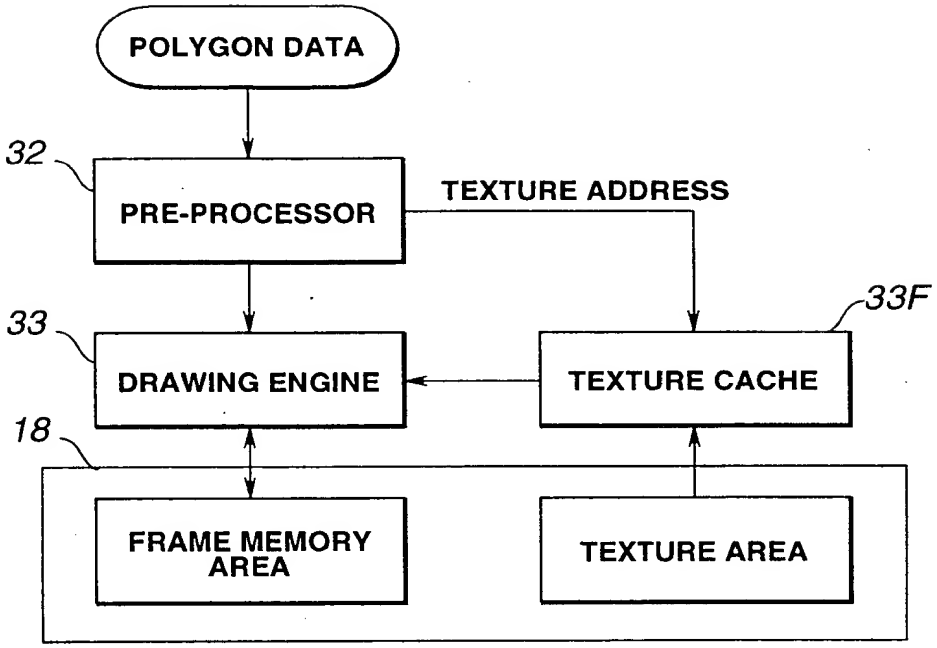
POLYGON DATA
32
PRE-PROCESSOR
TEXTURE ADDRESS
33
33F
DRAWING ENGINE
TEXTURE CACHE
18
FRAME MEMORY AREA
TEXTURE AREA

FIG.3


TAG
DATA
L

FIG.4

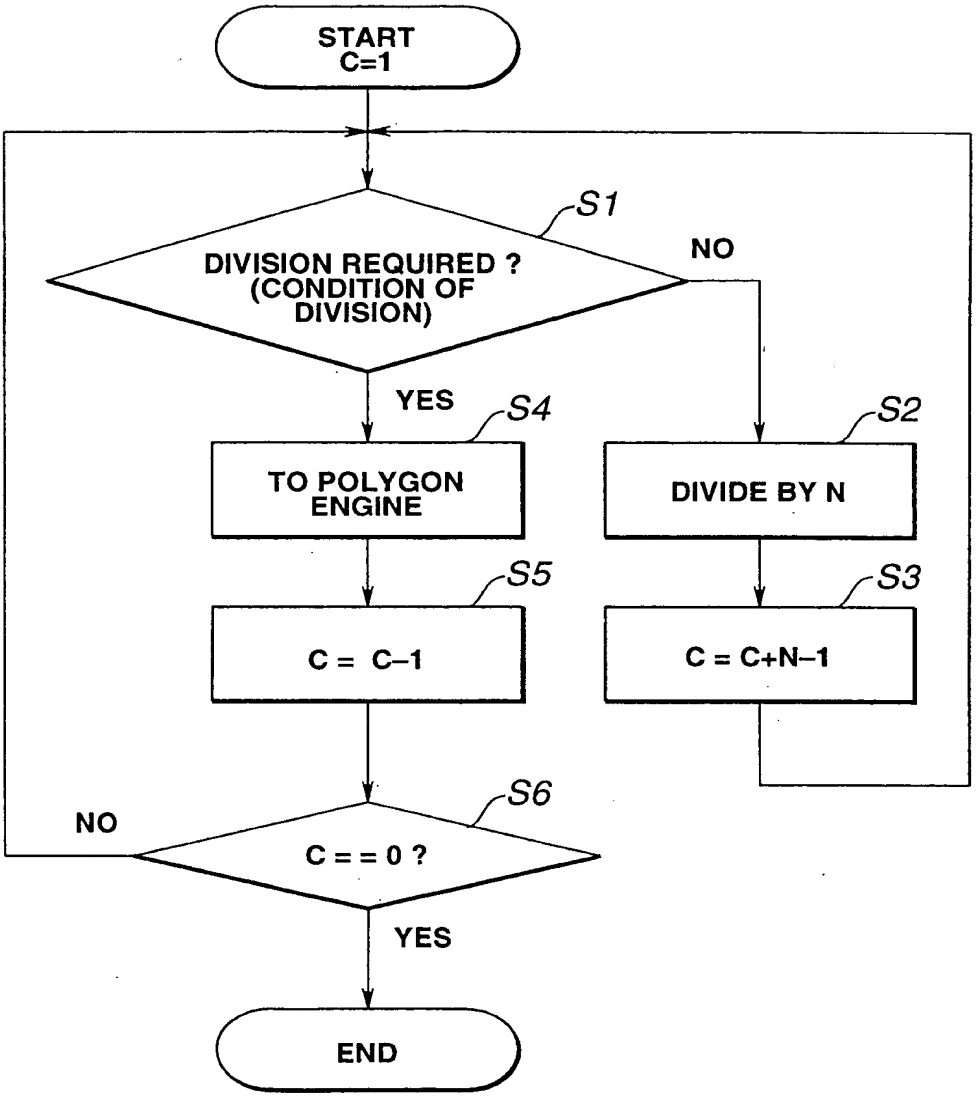
START
C=1
S1
DIVISION REQUIRED ?
(CONDITION OF
DIVISION)
NO
YES
S4
TO POLYGON
ENGINE
S2
DIVIDE BY N
S5
C = C–1
S3
C = C+N–1
S6
NO
C = = 0 ?
YES
END

FIG.5

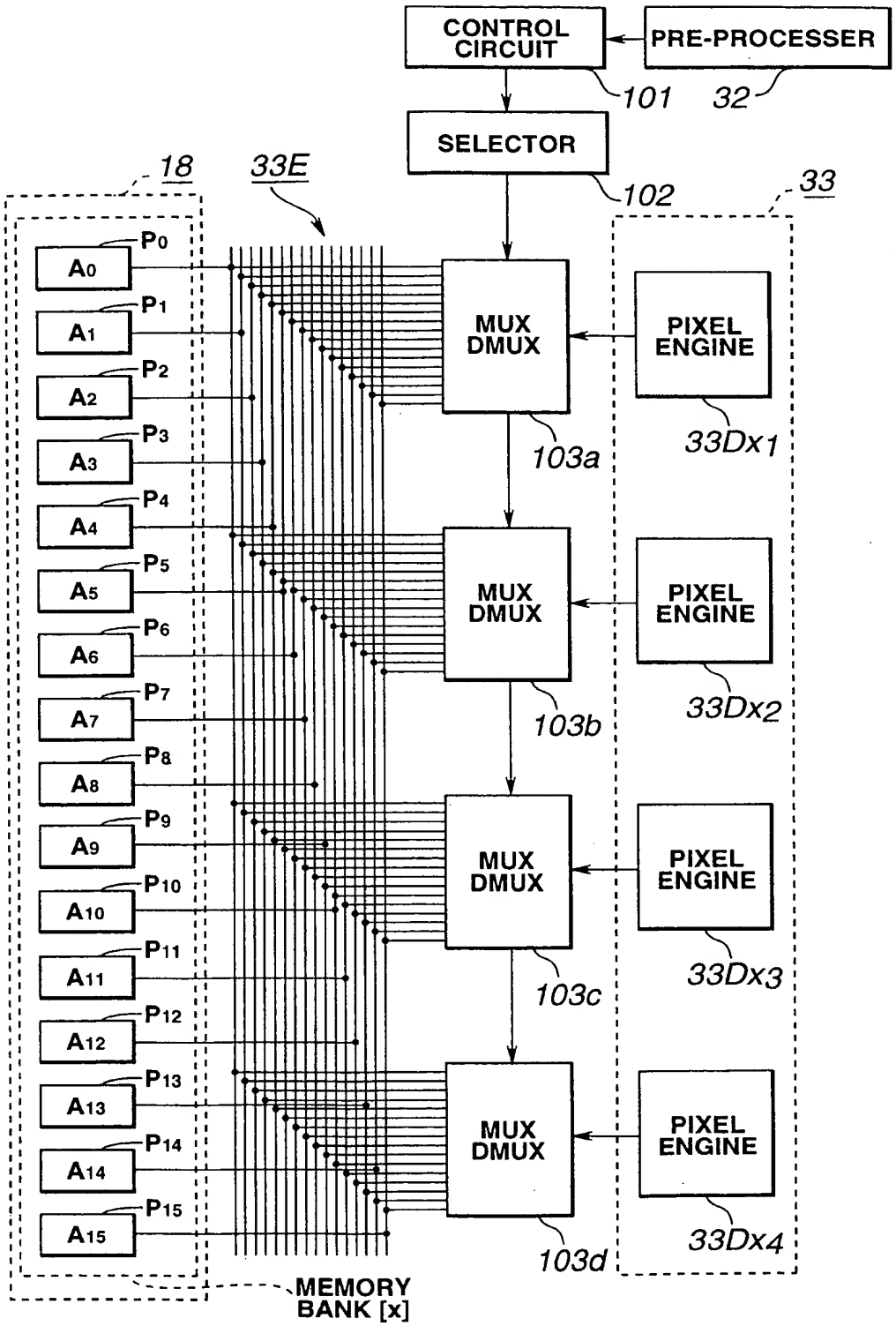
CONTROL CIRCUIT
PRE-PROCESSER
101
32
SELECTOR
102
18
33E
33
P0
A0
P1
A1
P2
A2
P3
A3
P4
A4
P5
A5
P6
A6
P7
A7
P8
A8
P9
A9
P10
A10
P11
A11
P12
A12
P13
A13
P14
A14
P15
A15
MUX DMUX
MUX DMUX
MUX DMUX
MUX DMUX
PIXEL ENGINE
PIXEL ENGINE
PIXEL ENGINE
PIXEL ENGINE
103a
103b
103c
103d
33Dx1
33Dx2
33Dx3
33Dx4
MEMORY BANK [x]

FIG.6

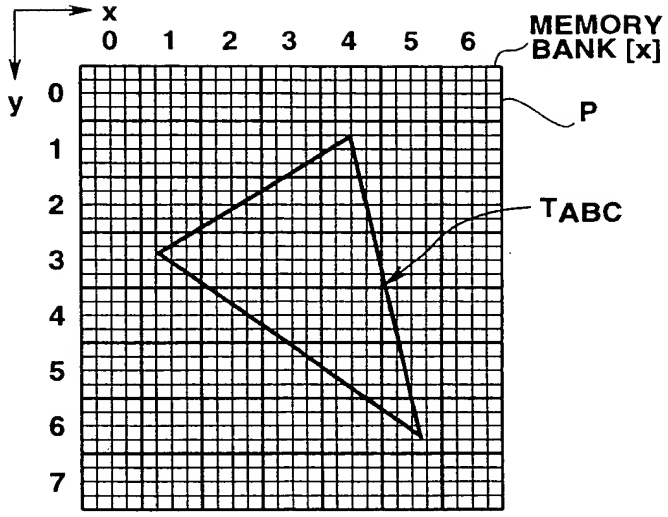

FIG.7

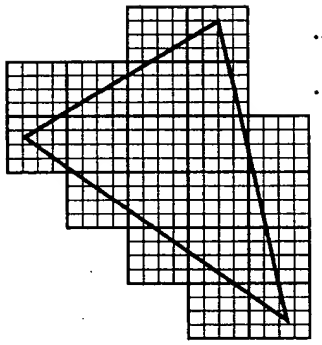

FIG.8

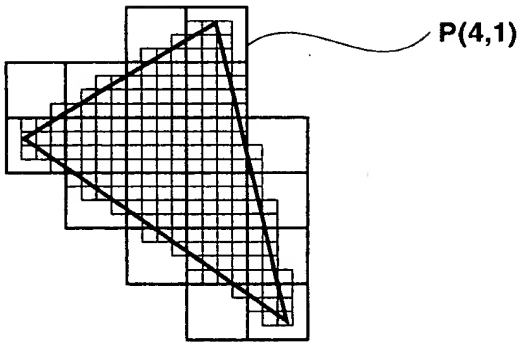

FIG.9

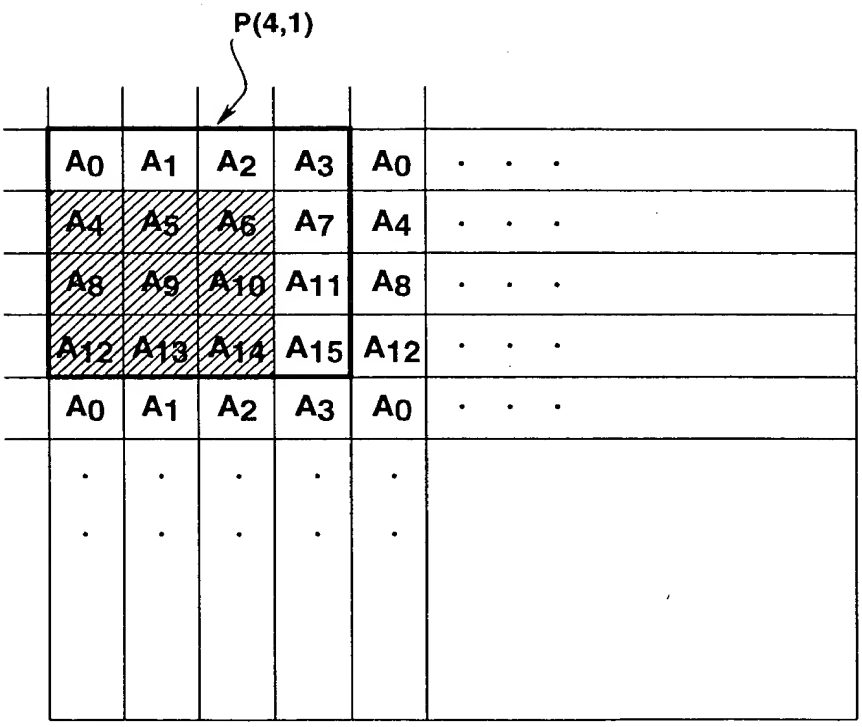
P(4,1)
A0 A1 A2 A3 A0
A4 A5 A6 A7 A4
A8 A9 A10 A11 A8
A12 A13 A14 A15 A12
A0 A1 A2 A3 A0

FIG.10

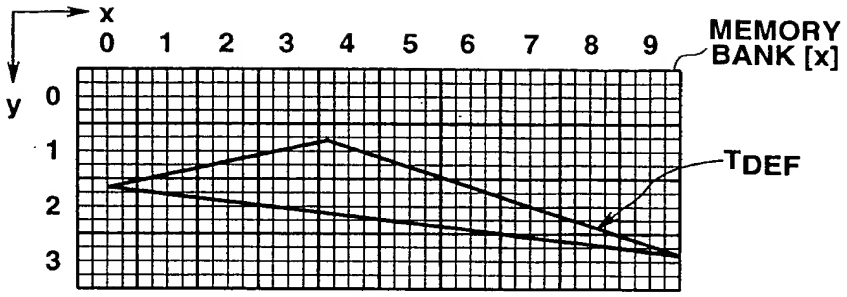

FIG.11

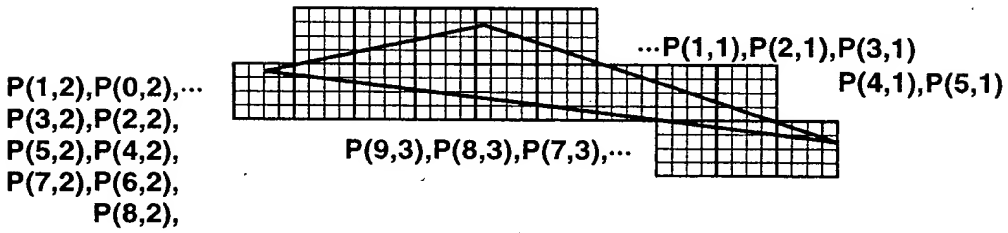

FIG.12

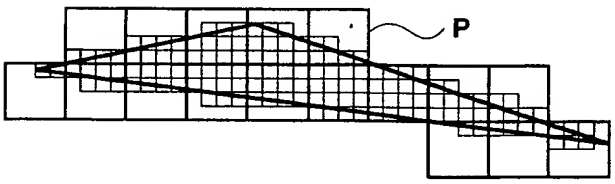

FIG.13

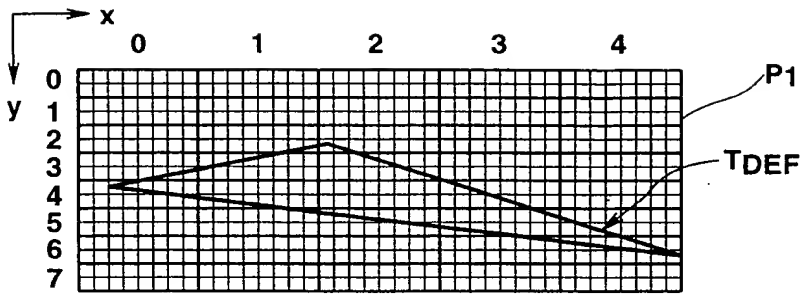

FIG.14

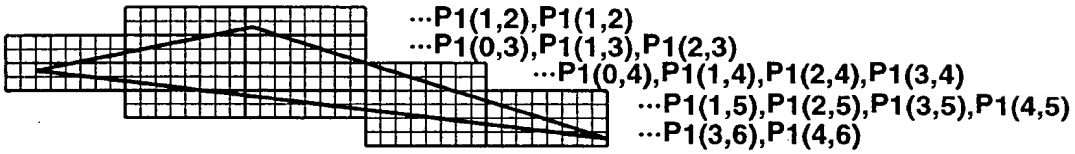

FIG.15

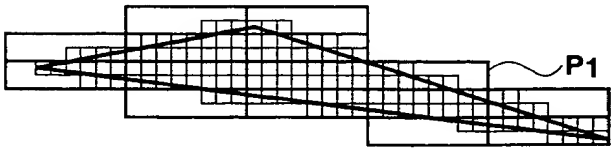

FIG.16

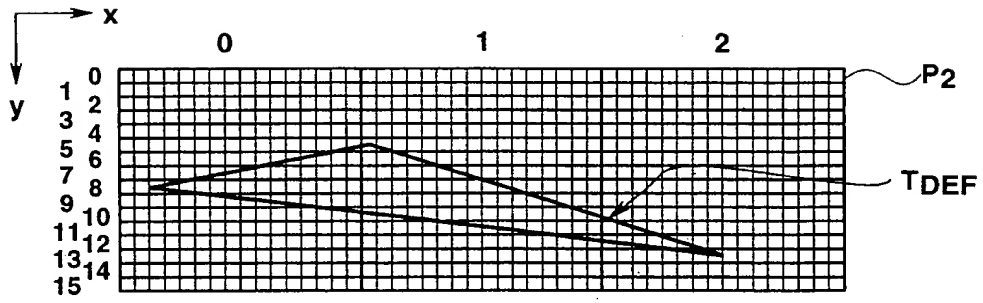

FIG.17

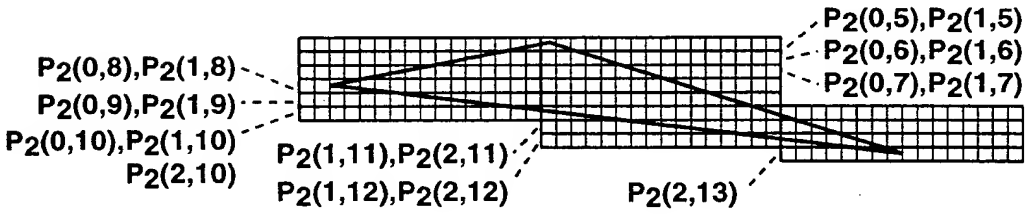

FIG.18

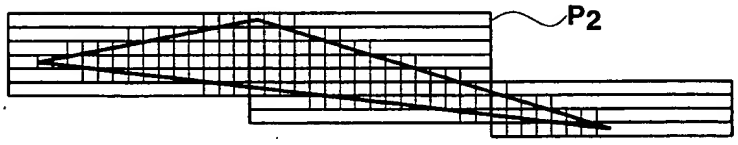

FIG.19

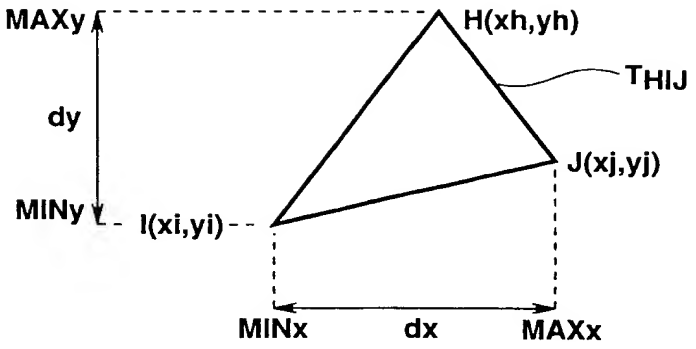

FIG.20

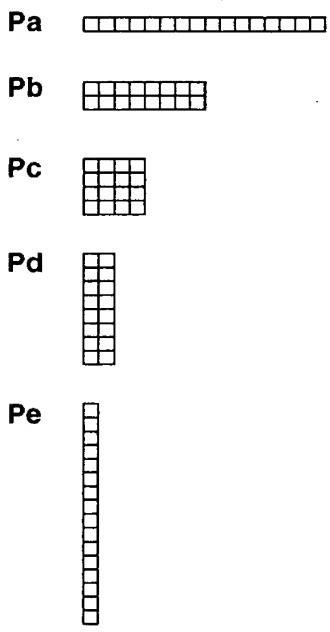

FIG.21

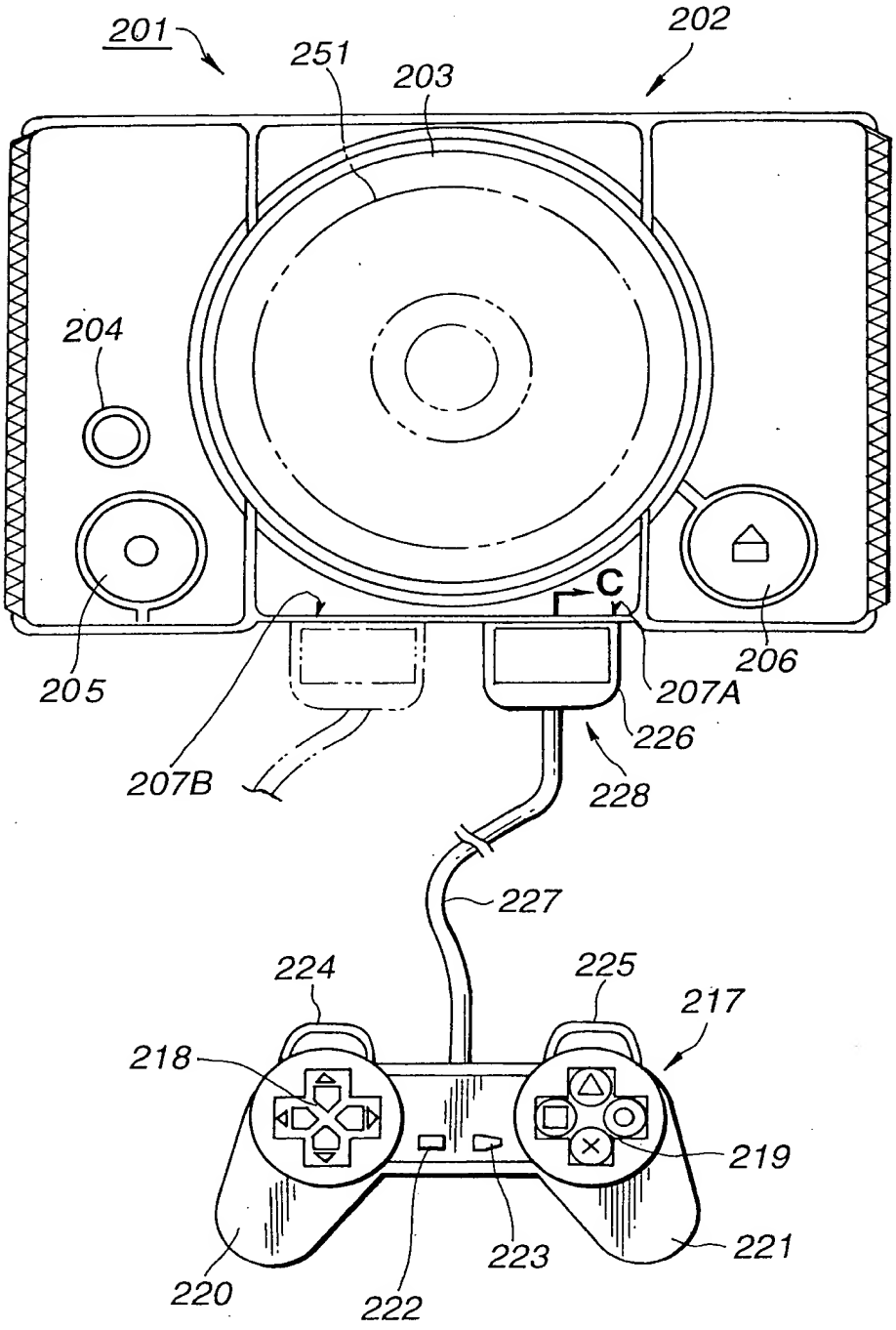
201
251
203
202
204
205
C
206
207A
207B
226
228
227
224
225
217
218
219
221
220
222
223

FIG.22

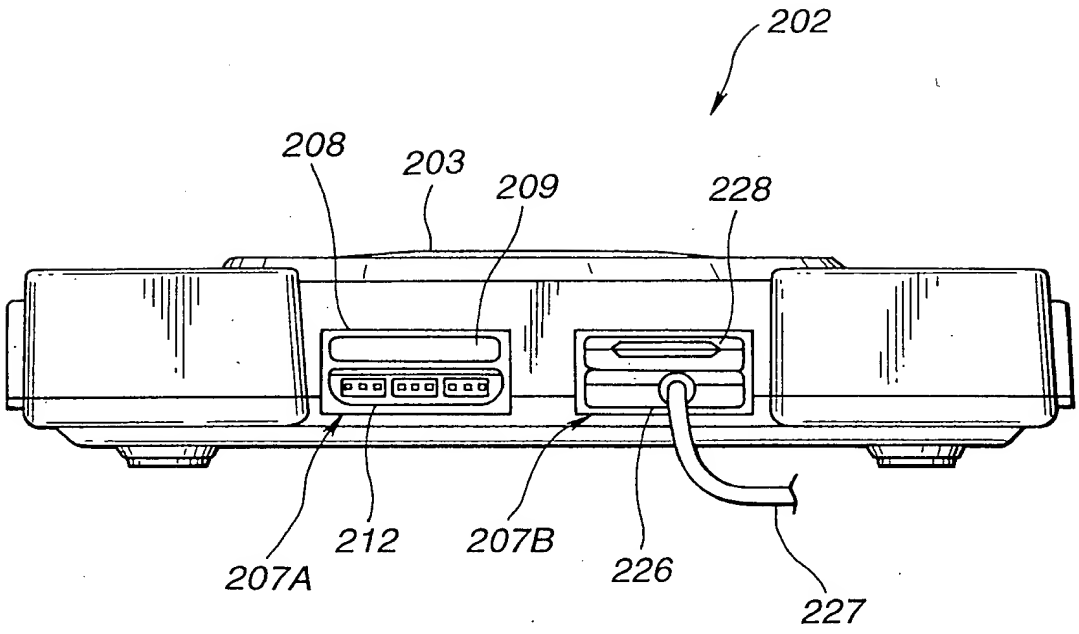

FIG.23

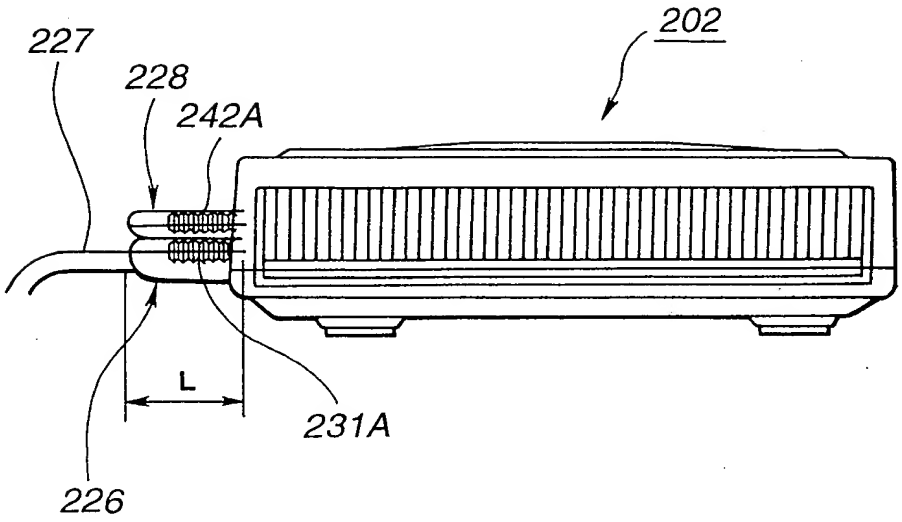

FIG.24

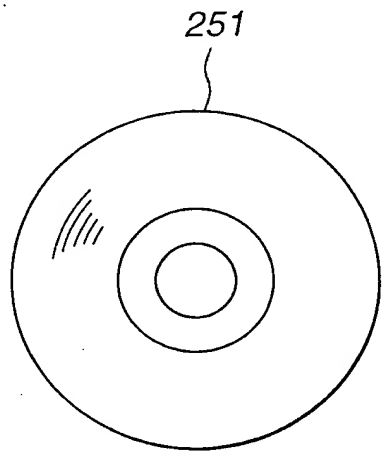

FIG.25